MOTOROLA

Microprocessors and Memory
Technologies Group

M68SC302ADS

Application Development System User's Manual

Revision 1.0

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SECTION 1
INTRODUCTION

This manual provides general information, preparation for use and installation instructions, operating instructions, functional description, and support information for the M68SC302 Application Development System board.

1.1 FEATURES

The main features of the M68SC302ADS board are as follows:

- MC68SC302 operating @20.48Mhz.
- Host computer interface with ISA Bus or PCMCIA bus.
- ISA PnP Interface supporting 8 and 16 bit memory and IO accesses.
- Option for three types of serial EEPROM for the PCMCIA or ISA Configuration.
- Powered by the ISA, PCMCIA connectors or external power connector.
- A complete connectivity with 2B1Q for connection to U interface.
- The U interface transceiver MC145572 interfaced to the M68SC302 either by IDL or GCI interface (selectable).Can be configured in NT or LT mode.
- The U interface transceiver MC145574 interfaced to the M68SC302 either by IDL or GCI interface (selectable). Can be configured in TE or NT mode.
- The S/T interface transceiver MC145574 used as a Master TE or NT interfaced to the M68SC302.
- The MC68SC302 can set up to have its system clock provided by the by the MC145572 BUFEXTAL output requiring only one crystal in the system.
- The S/T transceiver can use the M68SC302 system clock for its system clock requiring only one crystal in the system.
- Logic analyzer connectors compatible to probe M68SC302 activity and some of the S/T and the U transceivers signals.
- 128 pin expansion connector provides access to all of the MC68SC302 pins and to most of the S/T and U transceivers pins.
- Status LEDs for ISA bus, PCMCIA bus, RXD, TXD, S/T interface running, U interface running, and S/T loop-back.

1.2 GENERAL DESCRIPTION

The M68SC302ADS is a development tool for the MC68SC302 device. Figure 1-1 shows the block diagram of the board. This board is intended for hardware and software development of applications using the MC68SC302 Passive ISDN Protocol Engine (PIPE).

The M68SC302ADS can be connected to ISA Bus or PCMCIA Bus. It provides compatibility with both ISDN basic rate layer 1 interfaces: S/T (M145574) and U (M145572). Jumpers and

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dip switch setting provide flexibility to configure these interfaces in most of their supported modes.

The M68SC302ADS has logic analyzer connectors and expansion connectors, providing physical connection to all pins of the SC302 on the board. The logic analyzer connectors enable access to the bus activity and the I/O pins of the SC302, and some of the S/T and U transceivers pins. The expansion connector is located at the top of the board and provides most of the M68SC302 signals and some important transceiver signals. This connector is intended to be used as a connector for user specific breadboards or daughter cards for functions such as modems and POTs interfaces.

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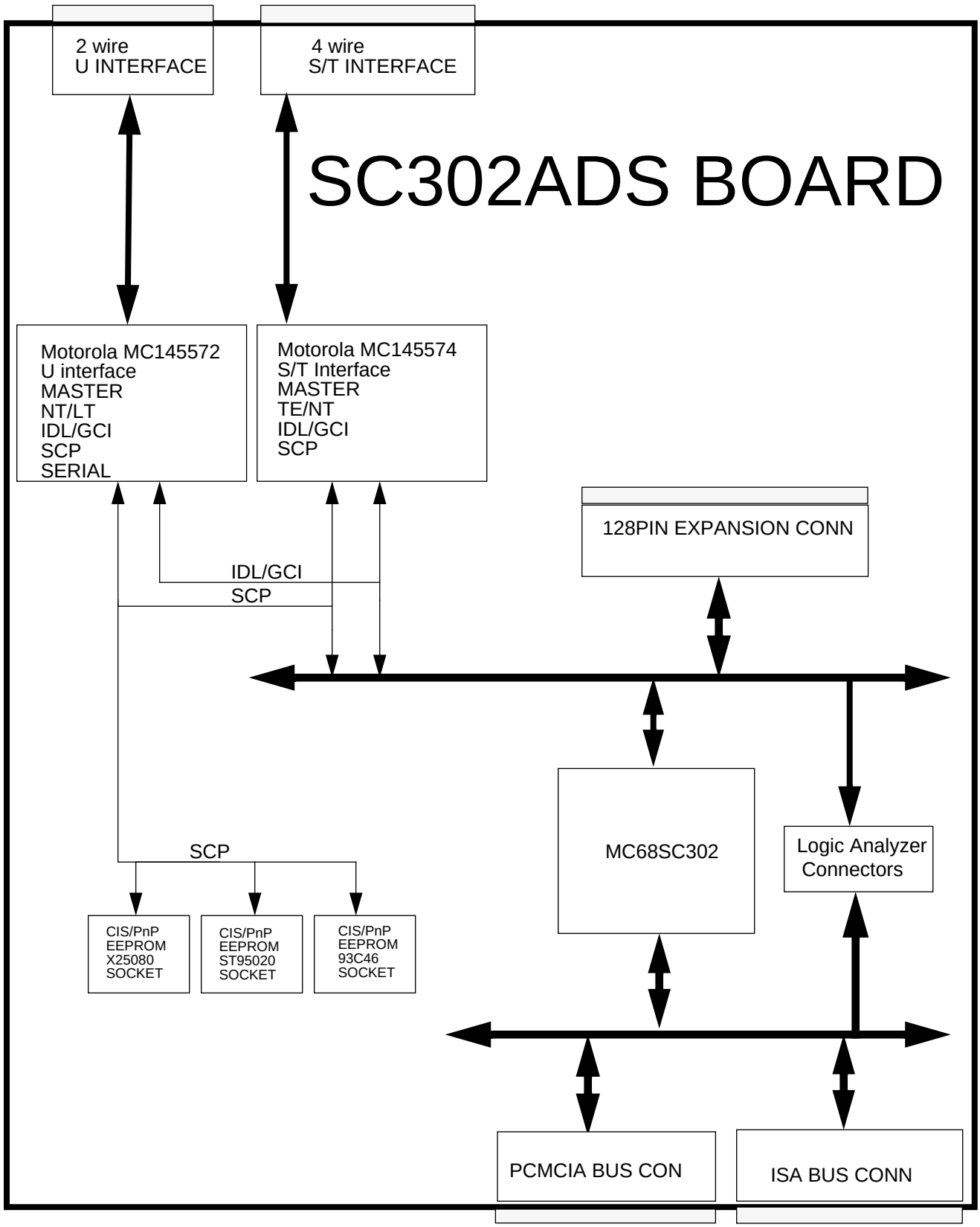
Figure 1-1. 68SC302ADS Block Diagram



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1.3 RELATED DOCUMENTATION

The following publications are applicable to the M68SC302ADS and may provide additional helpful information.

- M68SC302 User's Manual.
- MC145572 U interface User's Manual.
- MC145574 S/T interface User's Manual.
- ISA and EISA theory and operation, Edward Solari, ISBN 0-929392-15-9.
- The PC Card Standard, PCMCIA Association, 408-433-CARD
- Plug and Play Specification, Intel Corporation

1.4 ABBREVIATIONS USED IN THE DOCUMENT

- SC302 - ISDN Passive ISDN Protocol Engine (PIPE).
- ADS - Application Development System board.
- U Interface -The physical access point to the ISDN at the U reference point.
- S/T Interface - The physical access point to the ISDN at the S, T reference points.
- SC302ADS - Application Development System for the SC302 device.
- GCI - General Circuit Interface.
- SCP - Serial Communication Port.
- IDL - Interchip Digital Link.
- NT - Network Termination.
- LT - Line Termination.
- TE - Terminal Equipment.
- PnP - Plug And Play.
- ISA - Industry Standard Architecture.
- PCMCIA - Personal Computer Memory Card International Association.
- CIS - Card Information Structure.
- ISDN - Integrated Service Digital Network.
- spec - Engineering specification document.
- NMI - Non Maskable Interrupt.

1.5 REQUIRED EQUIPMENT

The M68SC302ADS can operate in two working environments:

- ISA bus.
- PC Card 95 type II card slot.

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SECTION 2
CONFIGURATION AND INSTALLATION

2.1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the M68SC302ADS.

2.2 UNPACKING INSTRUCTIONS

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

2.3 SET DIP SWITCHES AND JUMPERS

Before installing the board in the target machine it is necessary to verify that the dip switch and jumper settings on the board are correct for the users desired application. The following paragraphs describe these settings and some common configurations.

The locations of the dip-switches, and jumpers can be found by referring to Figure 2-1. The board is shipped with dip-switch settings as shown in the “default” column of Table 3-1, Table 3-2, Table 3-5, and Table 3-6. With the default dip switch settings all IRQ (DS1) pins are connected to the ISA bus. The U transceiver (DS2) is configured as NT, IDL, MASTER. The power up reset circuit is unconnected and the reset is connected directly to the ISA bus (DS4). The board is configured as an ISA card.

2.3.1 Selecting ISA mode

The board is shipped with DS4 Switch 8 in the “ON” position which configures the SC302 pins for ISA mode. If the board is going to be used in ISA bus mode verify that DS4 Switch 8 is ON. This will configure the 68SC302 pins on RESET to their ISA mode functions.

2.3.2 Selecting PCMCIA mode

If the board is going to be used in PCMCIA bus mode switch DS4 Switch 8 is OFF. This will configure the 68SC302 pins on RESET to their PCMCIA mode functions.

2.3.3 Selecting the SC302 clock source

The board has three options for providing a system clock to the Extal pin of the 68SC302:

1. The board is shipped with parts installed for the 68SC302 to source its clock from the 20.48MHZ dedicated crystal oscillator (X2).
2. A clock oscillator (U18) can be used. In order to use the clock oscillator, C33, X2, R36, and R38 must be removed from the board. Install a Clock SC Oscillator which complies with the electrical specifications of the 68SC302 (see M68SC602 User’s manual for specifications).
3. If the MC145572 U transceiver is used in the application, it can provide a 20.48MHZ clock to the 68SC302 from its BUFXTAL pin. To connect the MC155572 BUFXTAL pin

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to the SC302 EXTAL pin, remove the zero ohm resistor from R35 and remove the 100 ohm resistor from R38, and install a zero ohm resistor in R37.

2.3.4 ISDN Transceiver and Line Interface Setup

There are two DIP switches that need to be setup for ISDN line transceiver and interface selection (DS2 and DS3). Refer to Section 3 Design information for information on how to configure these Dip Switches. The board is shipped from the factory configured as described below.

2.3.5 Selecting the U interface in master mode, NT mode, IDL, SCP (MCU mode) - Default

Table 2-1 shows the dip switch and jumper selections for setting up the card to run in NT mode, IDL master mode, and using the SCP. The board is shipped from the factory with these settings. PA3(SCPEN3) is connected to the U interface $\overline{\text{SCPEN}}$ pin.

Table 2-1. Dip switch settings for U interface in master mode, NT mode, IDL, SCP

SWITCH	1	2	3	4	5	6	7	8
DS2	1	1	1	1	0	0	0	X
DS3	X	0	X	X	X	X	X	X

Dip switch settings: 1= on 0 =off X= Don't care

2.3.6 Serial EEPROM

2.3.6.1 ISA SERIAL EEPROM INSTALLATION. The board is shipped from the factory with two serial ISA mode serial EEPROMS. An ISA IO mode serial EEPROM is installed in either U4 or U11depending on the type (U4 is a 9346 type, and U11 is a 25XX or 95XX SPI type EEPROM). A ISA memory mode EEPROM is also included. At the time of printing all Motorola factory support software is for ISA IO mode accesses.

2.3.6.2 PCMCIA SERIAL EEPROM INSTALLATION. For PCMCIA applications it is necessary for the user to remove the supplied ISA mode serial EEPROM (U4 or U11) and provide their own programmed serial EEPROM for the CIS (it is recommended to use a 25XX or 95XX SPI type serial EEPROM installed in U11). Please refer to the 68SC302 User's Manual for information on creating the CIS for this EEPROM.

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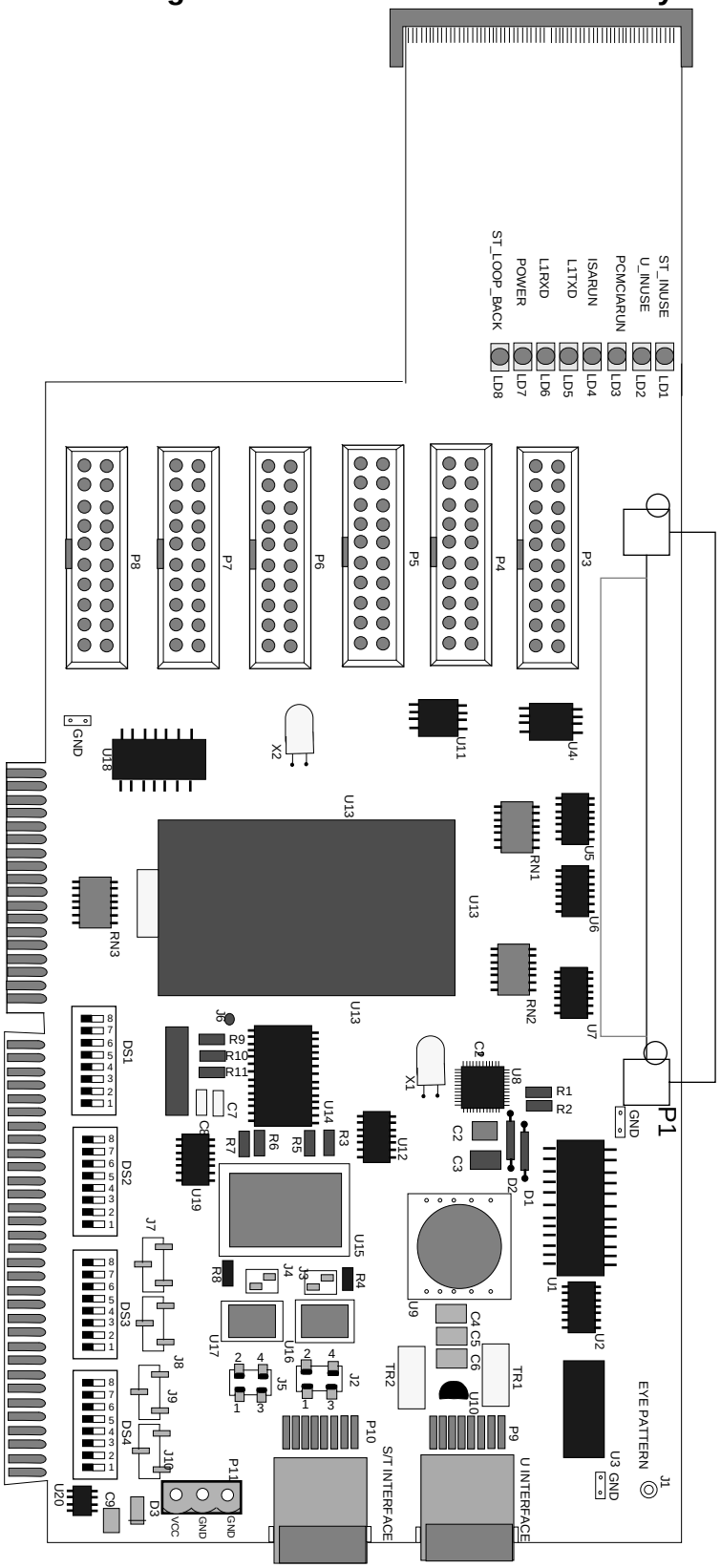
Figure 2-1. M68SC302ADS Parts Layout



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2.3.7 Installing the board in the system

2.3.7.1 ISA BUS.

1. Insure that the PC is turned off.
2. Plug the ISA card into a free ISA slot (Figure 2-2).
3. Turn on the PC.

2.3.7.1.1 Tips on accessing the card in a Windows 95 PNP system.

1. When Windows 95 starts up, it will detect the card and display a dialog box saying that it has detected new hardware. If you do not have a driver to load with the ADS card, you can pick the option to load one of the devices already shipped with Windows95 as a placeholder.

Note

We have had success at selecting the Motorola Bitsurfer in our versions of Windows95. This device does not seem to load any device driver (like VCOMM) that conflicts with our ability to directly address the assigned IO or memory space of the SC302ADS.

2. Verify that the card is loaded into the system by finding the device in the Device Manager in the System ICON in the Control Panel. Verify that the card was given the desired interrupt, memory or IO space. Note the locations for future reference. For the IO EEPROMS currently shipped with the ADS board, you should get a 4 byte internal IO space, this is for internal SC302 memory and register accesses. You will also get an external IO memory space for the external chip select.
3. You should now be able to access the card using SC302Bug from Motorola or the DOS debug command. A good way to verify that the card is installed properly in the PC is to turn on the one of the LEDs (see schematic in and 68SC302 users manual for PIO pins and register locations).

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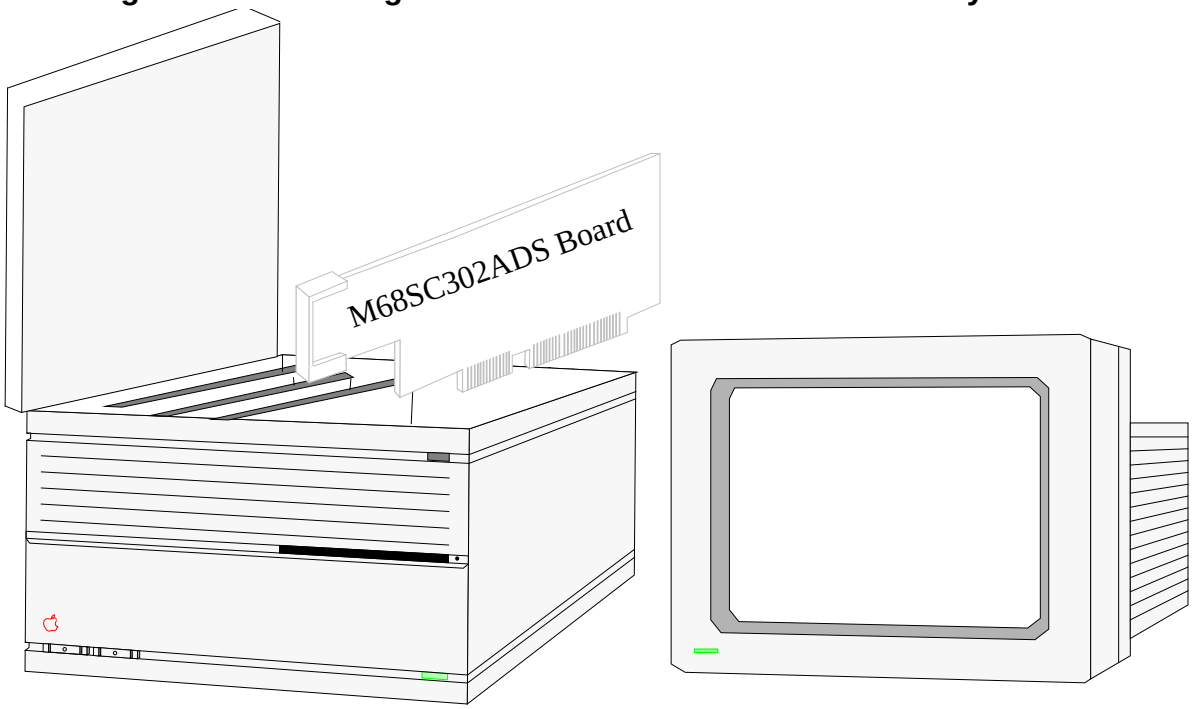
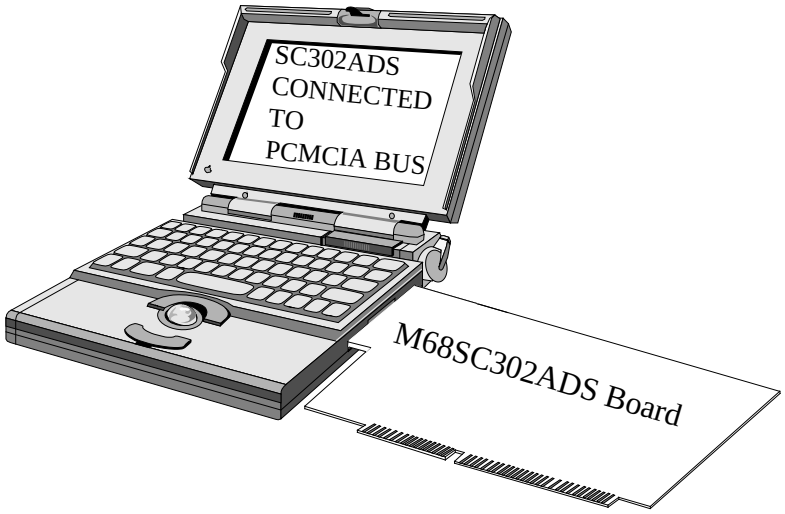
Figure 2-2. Installing the M68SC302ADS board in an ISA system.



2.3.7.2 PCMCIA BUS INSTALLATION.

1. Insure that the PC is turned off.
2. Plug the PCMCIA connector (P2) card into a free PCMCIA slot (Figure 2-3).
3. Turn on the PC.

Figure 2-3. Installing the M68SC302ADS in a PCMCIA slot



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SECTION 3
DESIGN INFORMATION

3.1 MC145572 U TRANSCEIVER

The MC145572 U interface transceiver is a single chip device for Integrated Services Digital Network, ISDN. The M68SC302ADS was designed to allow the MC145572 to be configured in most of its operating modes. DS2 are used to configure many of the options on the MC145572 as shown in Table 3-1.

Table 3-1. U Chip Configuration Dip Switch (DS2)

Number	ON	OFF	Default
DS2(1)	Connects the 68SC302 SCPRXD pin to the OUT2/SCPTX pin MC145572	Unconnected	ON
DS2(2)	Connects the 68SC302 SCPTXD pin to the OUT1/SCPRX pin MC145572	Unconnected	ON
DS2(3)	Connects the 68SC302 SCPCLK pin to the IN2/SCPCLK pin MC145572	Unconnected	ON
DS2(4)	Connects the 68SC302 PA3 pin to the IN1/ SCPEN pin MC145572	Unconnected	ON
DS2(5)	LT	NT	OFF
DS2(6)	FULL GCI **In full GCI mode DS2(1 - 4) must be OFF**	IDL **In IDL mode DS2(1 - 4) must be ON**	OFF
DS2(7)	For GCI mode only CLKSEL = 0, DCL = 512Khz	For GCI mode only CLKSEL = 1, DCL = 2.048Mhz	OFF
DS3(2)	SLAVE	MASTER	***OFF***

3.1.1 Selecting between S/T and U interface master

In order to allow the S/T and the U transceivers both to be mounted on the board, one device should be in Master mode and the other one should be in Slave mode.
In order to prevent any possibility of IDL/GCI bus contention. DS3 - 2 selects between the S/T and the U chip as master.

3.1.2 Selecting GCI vs. IDL on the MC145572

DS2 SW 6 selects between full GCI (ON) or IDL (OFF) modes. In IDL mode the U transceiver is controlled by the SCP port and in order to connect the 68SC302 SCP port to U chip SCP pins, DS2 SW 1,2,3,4 should be set to ON.

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3.1.3 Using GCI timing with SCP control on the MC145572

It is possible to be in IDL mode (DS2 SW 6 is OFF) and change the U transceiver to operate in GCI mode. The IDL interface is configured to accept GCI interface timing by setting MC145572 OR6(b3), GCI Mode Enable, to'1'. In this mode only 2B+D data is transferred between the MC145572 and GCI interface (SC302). The other bits in GCI interface are ignored. Four signal pins are available in this mode: DCL, FSC, Din and Dout. The control and status information for the MC145572 is provided through the SCP port. DCL is a 2X bit clock, Din accepts data from the IDL interface to be transmitted onto the U interface, Dout transmits data received from the U interface onto the IDL interface, and FSC is 8Khz frame synchronization pulse. Dout is driven only when 2B+D data is output from the MC145572. During all other bit times of GCI frame Dout is high impedance.

3.1.4 Selecting between NT and LT mode on the MC145572

DS2 SW 5 selects the U interface to be NT (OFF) or LT (ON) mode. Note that Byte Register 8 bit 0 also controls NT or LT mode selections.The SCP should be disconnected from the U interface if the MC145572 is configured in master GCI mode (DS3 SW 2 is OFF) (DS2 - 6 is ON) *(*DS2 SW 1 - 4 in the off position).

3.1.5 GCI mode clock rate selection on the MC145572

DS2 - 7 In full GCI the U-transceiver provides a 2.048Mhz or 512Khz on the CDL output. The frequency can be selected by DS2 - 7. When DS2 - 7 is ON the output clock is 512Khz and when DS2 - 7 is OFF the out clock is 2.048Mhz.
For more details on the U transceiver look at the MC145572 User Manual.

3.1.6 Clock Configuration options with the U transceiver

The board is supplied from the factory with the 68SC302 operating with a dedicated 20.48Mhz crystal connected through a zero ohm resistor (R35) to the EXTAL pin of the 68SC302. The MC145572 can drive the 20.48Mhz from the BUFXTAL on the MC145572 for NT U interface applications eliminating the necessity for two separate crystals. To set the board in this configuration remove R35 and mount a zero ohm resistor in the unpopulated R37 location.

3.2 MC145574 S/T TRANSCEIVER CONFIGURATION (DS3).

The MC145574 provides an economical VLSI layer 1 interface for the transportation of two 64kbps B channels and one 16kbps D channel between the network termination or NT and terminal equipment applications or TEs.The M68SC302ADS was designed to allow the MC145572 to be configured in most of its operating modes.

3.2.1 DIP Switch settings on the MC145574

The following are the DS2 DIP switch description. Table 3-2 also shows DS3 switch functions.

DS3 SW 1 This dip switch is for the T_IN/TFSC/TCLK/FIX pin. This pin performs four functions depending on the mode of operation. In all NT modes, except NT Terminal mode, this pin is the FIX input and enables the device to differentiate between fixed and adaptive

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timing modes. When DS3 - 1 is ON (low) the ADAPTIVE timing is selected and when DS3 - 1 is OFF (high) the FIXED timing is selected.

DS3 SW 2 This is the Master Slave select Dip Switch. This is a common dip switch for the S/T and the U transceiver's M/$\overline{S}$ input. This switch selects which transceiver will be the IDL or GCI master (provide the clocks). When this dip switch is ON, the S/T will be master and when this dip switch is OFF, the S/T will be slave. Conversely, when this dip switch is ON the U chip will be the slave and when in the OFF position the U chip will be the master.

DS3 SW 3 This dip switch is selects between TE or NT on the S/T chip. When the dip switch is ON the S/T will be in NT mode after S/T chip comes out of reset, and when the dip switch will be off the S/T will be in TE mode.

DS3 SW 4 This dip switch is for the GCI_SG/DGRANT/ANDOUT pin. DS3 - 4 is only for the NT Star mode to use the ANDOUT function. When using this mode DS3 - 4 should be OFF otherwise it should be ON.

DS3 SW 5 This dip switch is for the DREQUEST/ANDIN pin. DS3 - 5 is only for the NT Star mode to use the ANDIN function. When using this mode DS3 - 5 should be OFF otherwise it should be ON.

Table 3-2. DS3 functions

Number	ON	OFF	Default
DS3(1)	NT FIX	NT ADAPTIVE	ON
DS3(2)	S/T IS MASTER	U IS MASTER	ON
DS3(3)	NT	TE	ON
DS3(4)	NT TERM	NT STAR	OFF
DS3(5)	NT TERM	NT STAR	OFF
DS3(7)	NT TERM	NT STAR	OFF

3.2.2 Setting Jumpers J7, J8, J9 for the MC145574

J7, J8 and J9 allow the SC302 pins to be connected to the SCP pins of the MC145574 by connection pin 1 to pin 2 on each jumper. These pins on the MC145574 can be grounded by connecting pin 2 to pin 3 on each jumper. If a jumper is not installed the pins will be pulled up to 5Volts. This is useful for programming the GCI_DCL frequency and the channel number in GCI mode. Table 3-3 and Table 3-4 show the details of using these pins in GCI mode.

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Table 3-3. GCI NT master mode clock and channel selection

M2	M1	M0	GCI NT MASTER MODE
0	0	0	GCI_DCL = 2.048MHz, channel 0
0	0	1	GCI_DCL = 2.048MHz, channel 1
0	1	0	GCI_DCL = 2.048MHz, channel 2
0	1	1	GCI_DCL = 2.048MHz, channel 3
1	0	0	GCI_DCL = 1.536MHz, channel 0
1	0	1	GCI_DCL = 1.536MHz, channel 1
1	1	0	GCI_DCL = 1.536MHz, channel 2
1	1	1	GCI_DCL = 512KHz, channel 0

Table 3-4. GCI TE Master mode clock selection

M2	M1	M0	GCI MASTER MODE
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	GCI_DCL = 1.536MHz, Terminal node
1	0	1	Reserved
1	1	0	Reserved
1	1	1	GCI_DCL = 512KHz

3.2.3 Clock Configuration options with the MC145574 S/T transceiver

The board is populated at the factory with a dedicated crystal (X3) providing the clock to the MC145574 S/T chip EXTAL pin. It is possible to source the clock from the CLKOUT pin of the 68SC302 eliminating the need for the extra crystal dedicated to the MC145574. To implement a single crystal configuration on the 68SC302ADS board, remove R10 and populate R9 with a zero ohm resistor. You will also need to replace X2 with a 15.36MHZ crystal (you could use the one installed in X3).

3.2.4 Point to Point operation mode jumpers (J3, J4)

The J3 and J4 jumpers allow the MC145574 S/T to be operated in a point to point configuration. In the point to point mode of operation, one NT communicates with one TE.

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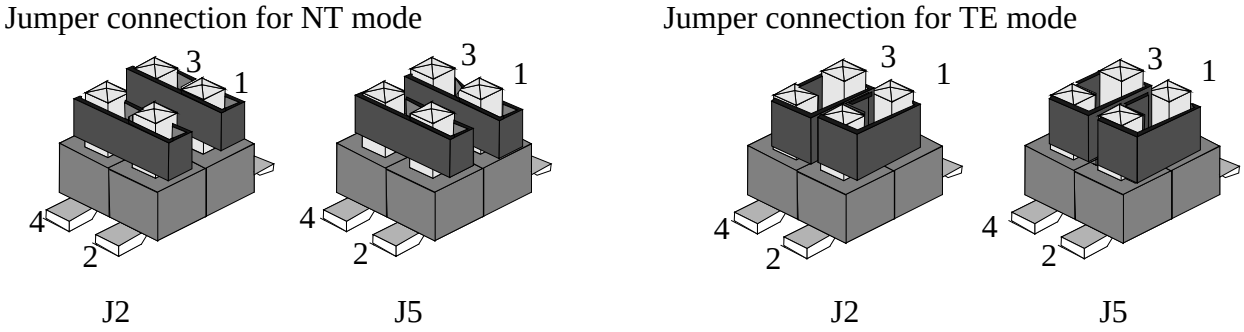
In this configuration, a 100 ohm termination must be connected across the transmit and receive paths of both the NT and TE transceivers. The jumpers connect the 100 ohm resistor to the transceiver line. The jumpers should be removed when connecting this board to an S/T network with more then on TE on it.

3.2.5 Selecting TE or NT on the ISDN S/T line interface (J2, J5)

TE and NT are connected differently on the RJ45 S/T connector (P10). For TE mode, pins 3,6 on P10 are the S/T transmit lines and 4,5 are the S/T receive lines. For NT mode, pins 3,6 on P10 are the S/T receive lines and 4,5 are the S/T transmit lines. If TE mode is selected, connect the jumpers on pins 1,2 and 3,4 on J2 and J5. If NT mode is selected, connect the jumpers on pins 1,3 and 2,4 on J2 and J5. This is shown in Figure 3-1.

Figure 3-1. J2, J5. Select TE or NT on the ISDN S/T connector



3.3 SC302 RESET OPTIONS

The M68SC302ADS board is supplied from the factory with the ISA reset and PCMCIA reset connected directly to the 68SC302 reset pin (DS4 SW 1 OFF). This should be sufficient in normal operation. However, for debugging purposes there is a power -on reset circuit that can be enabled by setting DS4 SW 1 in the ON position.

3.4 EYE PATTERN GENERATOR CIRCUIT

This circuit was designed into the card originally but is not populated because it is rarely used. Information on this circuit can be found in the Appendix D of the MC145572 User's Manual.

3.5 68SC302 CLKOUT TESTPOINT (J6).

J6 is a testpoint which is convenient for monitoring the SC302 CLKOUT pin.

3.6 IOCHRDY/IRQ5 JUMPER (J10)

This jumper is a three pin jumper. When pins 3 and 2 are bridged, the IOCHRDY is connected to the ISA Bus from the SC302. When pins 2 and 1 are bridged the IRQ5 is connected from the SC302 to the ISA Bus. The default is that IOCHRDY is connected.

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3.7 ISA IRQ DIP SWITCH (DS1)

The 68SC302 IRQs (IRQ3, IRQ9, IRQ10, IRQ11, IRQ12 and IRQ15) are connected to the ISA bus through DS1. DS1 allows the ISA IRQ pins to be disconnected from the 68SC302 multifunction pins so that the 68SC302 pins can be used for other functions.

Table 3-5.

Number	ON/OFF	Default
DS1(3)	IRQ9	ON
DS1(4)	IRQ15	ON
DS1(5)	IRQ12	ON
DS1(6)	IRQ11	ON
DS1(7)	IRQ10	ON
DS1(8)	IRQ3	ON

3.8 DIP SWITCHES DS4

DS4(1) when closed connects the power-on reset to the board and selects the desired operating bus for either ISA or PCMCIA. Table 3-6 details the purpose of each switch.

Table 3-6. Eye PAttern Decoder and Power Up Reset

Number	ON	OFF	Default
DS4(1)	Power On Reset Circuit enabled	Reset from ISA or PCMCIA bus	OFF
DS4(4)	Eye Pattern Circuit (See Schematic)		ON
DS4(5)			ON
DS4(6)			ON
DS4(7)			ON
DS4(8)	ISA Bus selected	PCMCIA Bus selected	ON

3.9 ST_INUSE (LD1)

LD1 is connected to the 68SC302 PA8 pin and can be used for any purpose but is often used to indicate that the MC145574 S/T interface is being used.

3.10 U_INUSE (LD2)

LD2 is connected to the 68SC302 PA5 pin and can be used for any purpose but is often used to indicate that the MC145572 U interface is being used.

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3.11 PCMCIARUN (LD3)

LD3 is connected to the 68SC302 PA11 pin and can be used for any purpose but is often used to indicate that the PCMCIA interface is being used.

3.12 ISARUN (LD4)

LD4 is connected to the 68SC302 PA10 pin and can be used for any purpose but is often used to indicate that the ISA interface is being used.

3.13 L1TXD LD5

LD5 is blinking when the SC302 L1TXD is active.

3.14 L1RXD LD6

LD6 is blinking when the SC302 L1RXD is active.

3.15 POWER LD7

LD7 is the power indicator for the SC302ADS board.

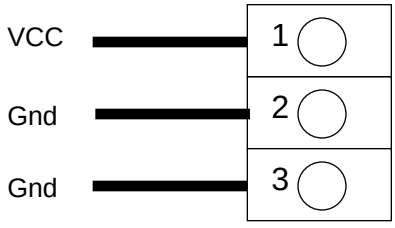
3.16 S/T LOOP BACK LD8

LD8 is lighted when the user is using the MC145574 internal loopback in both IDL and GCI modes.

3.17 +5V POWER SUPPLY CONNECTION

The M68SC302ADS requires +5 Vdc for operation. The SC302ADS can get its power supply from the ISA Bus connector or from the PCMCIA Bus connector or from P11 the external power supply connector. **NOTE**: P11 is not necessary for the normal operation of the board.
Connect the +5V power supply to connector P11 as shown below:

Figure 3-2. P11 +5V Power Connector



P11 is a 3 terminal block power connector with power plug. The plug is designed to accept 14 to 22 AWG wires. It is recommended to use 14 to 18 AWG wires. To insure solid ground, two Gnd terminals are supplied. It is recommended to connect both Gnd wires to the common of the power supply, while VCC is connected with a single wire.

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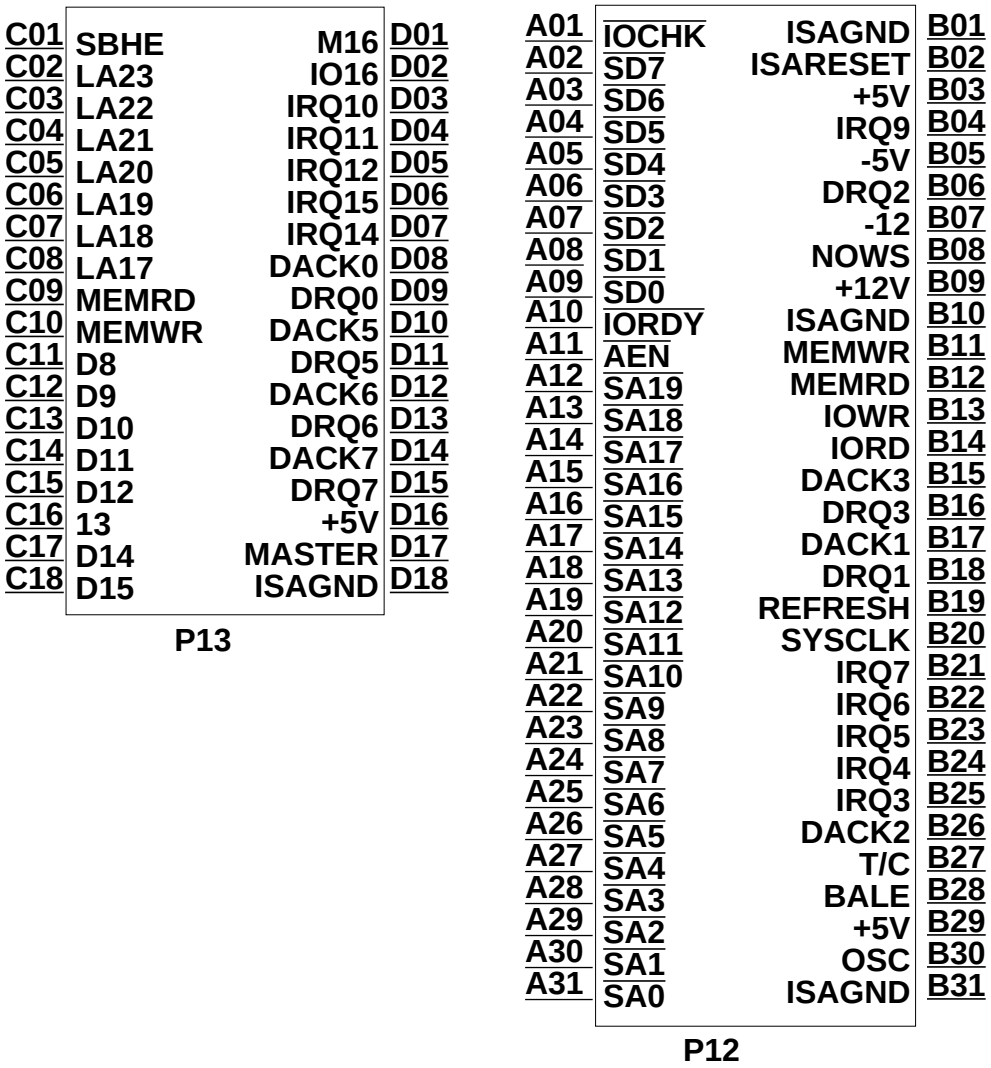
NOTE

Since hardware applications can be connected to the M68SC302ADS using the expansion connectors P1 and the additional power consumption should be taken into consideration when a power supply is connected to the 68SC302ADS.

3.18 ISA BUS CONNECTOR.

The ISA bus pinout is shown in Figure 3-3.

Figure 3-3. ISA BUS Connector



3.19 PCMCIA BUS

Figure 3-4 shows the PCMCIA connector pinout. DS4 SW 8 in the OFF position will enable the PCMCIA interface after 68SC302 reset. The PCMCIA interface is enabled by pulling

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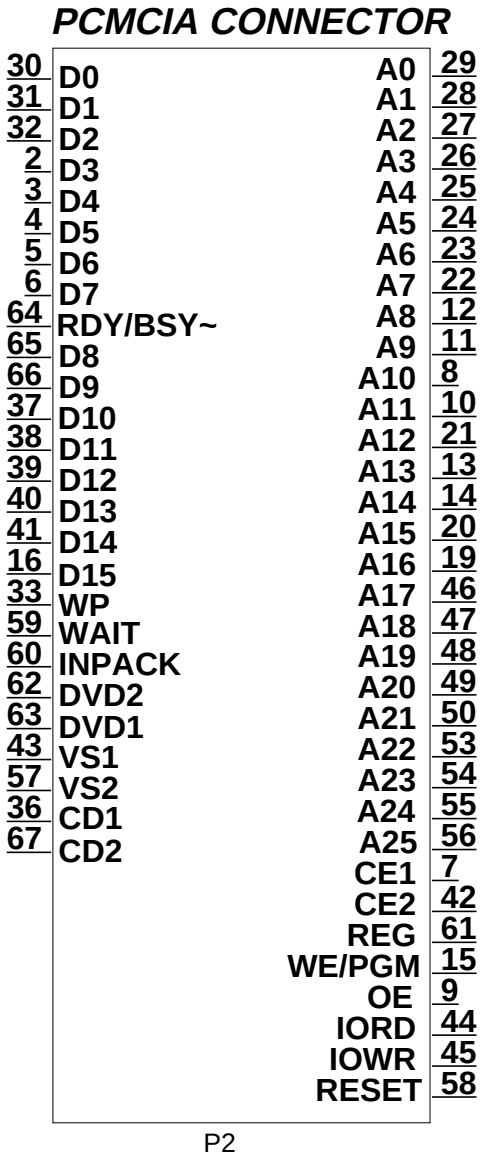
down the 68SC302 $\overline{\text{IOW}}$/$\overline{\text{PC_MODE}}$ pin low and pulling up the 68SC302 $\overline{\text{IOR}}$/PCE2E pin during 68SC302 reset.

Figure 3-4. PCMCIA Connector Pinout



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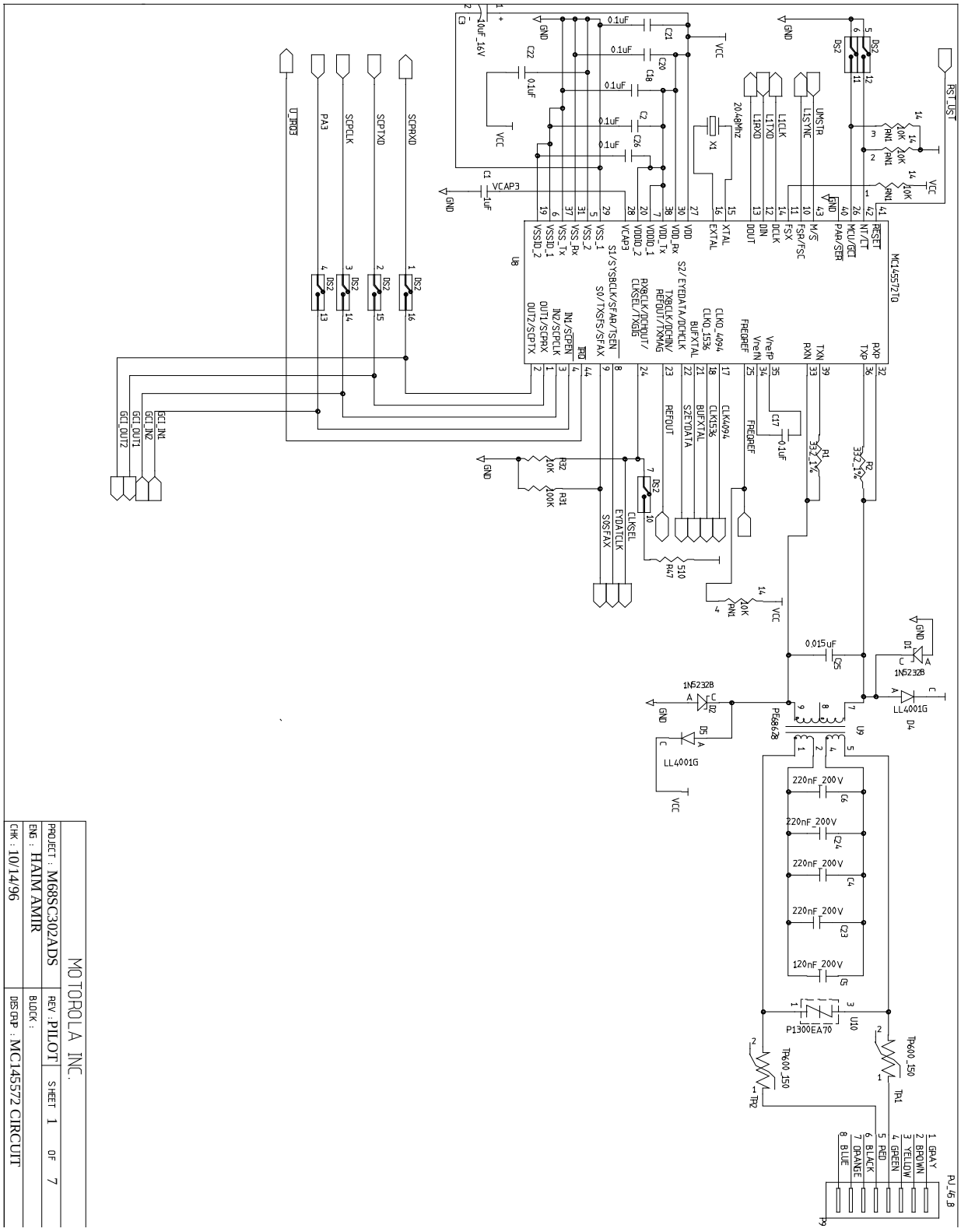
SECTION 4
SCHEMATICS

Figure 4-1. SHEET #1 MC145572 U Interface Transceiver.



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4.1 SHEET #1 MC145572 U INTERFACE TRANSCEIVER.

Sheet #1 shows the Motorola MC145572 U - Interface and all the necessary dip switches to configure it, with the exception of the M/S selection which is DS3(2) on sheet #2. The MC145572 reset is derived from the power up reset circuit, or from ISA/PCMCIA reset or from the SC302 PA9 signal. There is a logical OR between these two sources. DS2 handles the following MC145572 signals: DS2(5) selects the NT/LT mode: when DS2(5) is ON the MC145572 is in LT mode and when the DS2(5) is OFF the MC145572 is in NT mode.

DS2(6) selects the IDL/GCI mode, when DS2(6) is OFF the MC145572 is in IDL mode. When in IDL mode DS2(1 - 4) should be ON to connect the MC145572 SCP to the SC302 SCP. When DS2(6) is ON the MC145572 is configured for Full GCI mode the DS2(1-4) must be OFF. **NOTE**: In the case that DS2(6) is OFF, even when using the S/T only, DS2(1 -4) must be ON.

The MC145572 is configured for a serial device (PAR/SER signal connected to GND).Only one dip switch is selected to configure the S/T or the U to a master mode to prevent both interfaces from ever becoming the master at the same time. The UMSTR signal from sheet #2 is the inverse of the S/T M/$\overline{S}$ pin and is connected to the U interface. In master mode the MC145572 outputs the FSX and FSC in the same wave form, so the FSX is not needed and the pin is pulled up. FSX is not used in GCI mode, so only the FSC pin is used to synchronize the IDL and GCI frames.

L1SYNC, L1CLK, L1TXD and L1RXD are the SC302 signals used for the IDL and GCI buses.The MC145572 SCP pins are SCPEN, SCPCLK, SCPTX and SCPRX and these pins are used in IDL mode. These pins are not used in full GCI mode. In GCI mode these pins are IN1, IN2, OUT1 and OUT2. In full GCI mode, DS2(1-4) should be OFF and these signals can be accessed at the expansion connector for other applications.

The MC145572 has an IRQ pin to use in IDL mode and is connected to the SC302 PA6 pin on sheet #3. The CLKSEL signal has a dip switch to select the DCLK frequency in GCI mode: If CLKSEL is'0' (DS2(7) is OFF), the U transceiver DCLK frequency is 512khz and if CLKSEL is'1' (DS2(7) is ON), the U transceiver DCLK frequency is 20.48Mhz. The CLK4094, CLK1536, REFOUT and FRQREF signals are connected to the expansion connector to enable the user to use these pins.

BUFXTAL signal is the MC145572 buffered XTAL signal, it is connected to R37 on sheet #3 which is a 0 ohm resistor(unpopulated). This resistor can be populated to allow the MC145572 to drive the SC302 EXTAL from the BUFXTAL signal. Before mounting this resistor, R35 must be removed to prevent contention between the crystal signal and the BUFXTAL signal.

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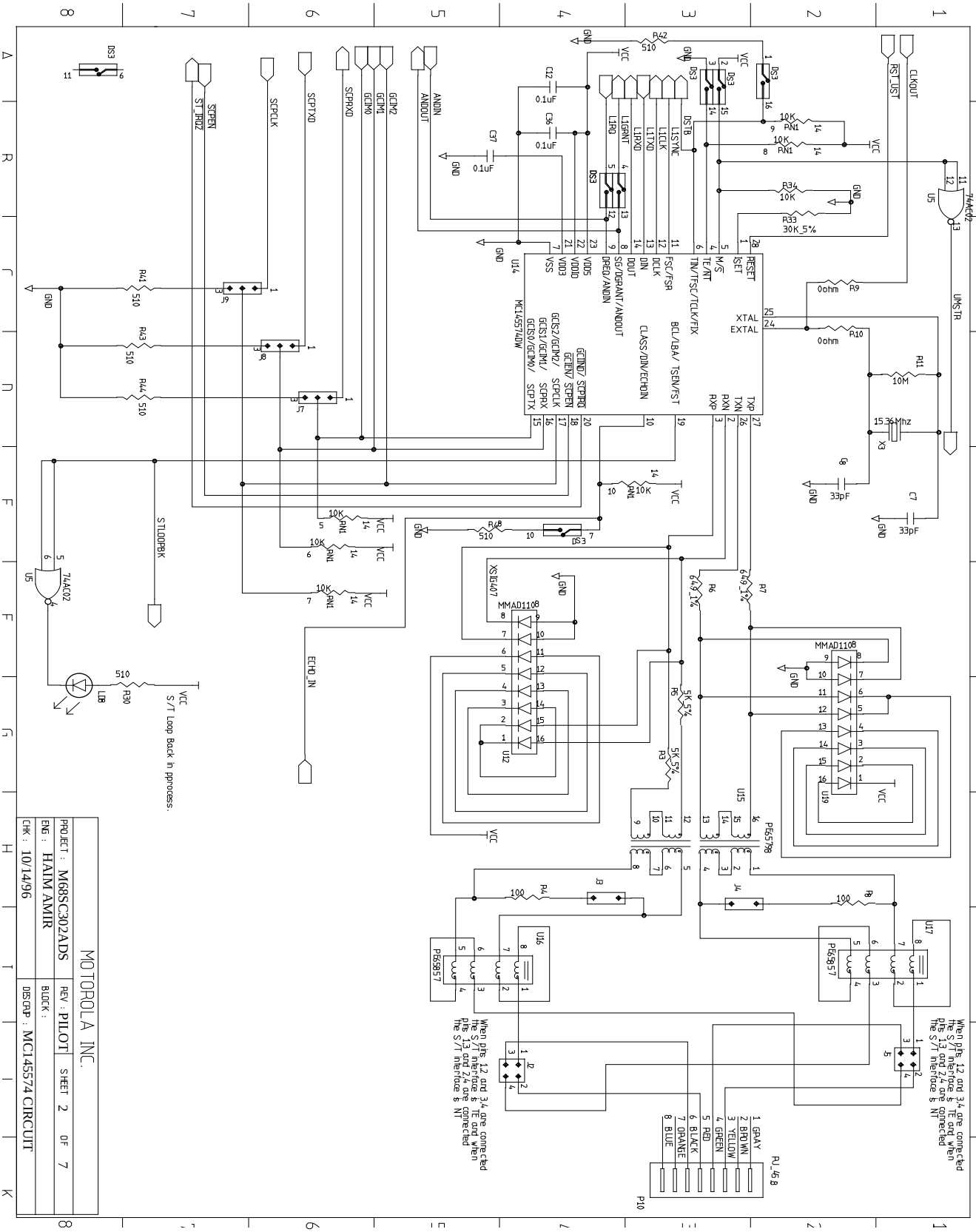
Figure 4-2. SHEET #2 MC145574 S/T Interface Transceiver.



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4.2 SHEET #2 S/T INTERFACE TRANSCEIVER.

Sheet #2 has the MC145572 S/T interface transceiver and related circuitry. The MC145574 reset is derived from either the power up reset, the ISA/PCMCIA reset or from the SC302 PA9 signal. Only one dip switch configures the S/T or the U transceiver master mode. When the S/T is in master mode, the U is in slave mode. The UMSTR signal goes to sheet #1 to select the U interface to be Master or Slave. This prevents the U chip and the S/T chip from both driving the DCLK, L1SYNC and DOUT signals at the same time. DS3(3) is configures the S/T to NT or TE. If set to on, the S/T will be in NT mode, if off the S/T will be in TE mode. DS3(1) is for NT mode, and selects between fixed and adaptive timing modes on the S/T. The DSTB signal is connected to logic analyzer connector and to the expansion connector for user applications. The DSTB is the D channel Strobe signal. When in TE MASTER mode this signal will transition to high during the time when the D bits are being input to the IDL_IN pin. L1SYNC, L1CLK, L1TXD and L1RXD are the IDL and GCI bus signals. DS3(4, 5) are enables to use the MC145574 in NT Star mode applications. In the NT Star mode DS3(4, 5) should be off to use the signals ANDIN and ANDOUT. in all other modes the DS3(4,5) should be on to use the L1GRNT and L1RQ signals.

J7, J8 and J9 are used to enable the use of all the functions of the GCIS0/GCIM0/SCPTXD, GCIS1/GCIM1/SCPRXD and GCIS2/GCIM2/SCPCLK signals. In IDL mode, pin 1 and 2 should be connected. In GCI INDIRECT mode these jumpers can select the Time Slot Assignment. In GCI Direct mode they can select the GCI_DCL frequency for NT or TE Master mode.The SCPEN signal is connected to the SC302 PA1/SCPEN1 pin and is the enable pin for SCP. This pin also enables the GCI to be in GCI direct mode. When this pin is low during MC145574 reset, the MC145574 will power up in GCI Direct mode.

CLASS/DIN/ECHOIN PIN DS3(7) is used in TE mode. The CLASS input used to determine the D_Channel access class. In NT terminal mode this pin is the D_IN input. D-channel data is input on this pin. In NT star mode, this pin is the ECHO_IN input for use in NT star applications. The ECHO_IN signal is connected to the logic analyzer connector and to the expansion connector.

R9 and R10 are 0ohm resistors. R10 is populated and R9 unpopulated. In normal operation, the MC145574 is clocked by the 15.36Mhz crystal. It is possible to clock the MC145572 by the SC302 CLKOUT signal. This should be a 15.36MHZ clock signal only. When using the SC302 CLKOUT signal R10 should be removed and R9 should be mounted. J3 and J4 connect or unconnect the 100 ohm termination.When operating in TE mode, only one TE should have the 100 ohm termination resistors in the transmit and receive paths. J2 and J5 are jumpered differently for NT and TE mode. For TE mode, pin 1 should be bridged to pin 2, and pin 3 should be bridged to pin 4 on both J2 and J5. For NT mode, pin 1 should be bridged to pin 3, and pin 2 should be bridged to pin 4 on both J2 and J5.

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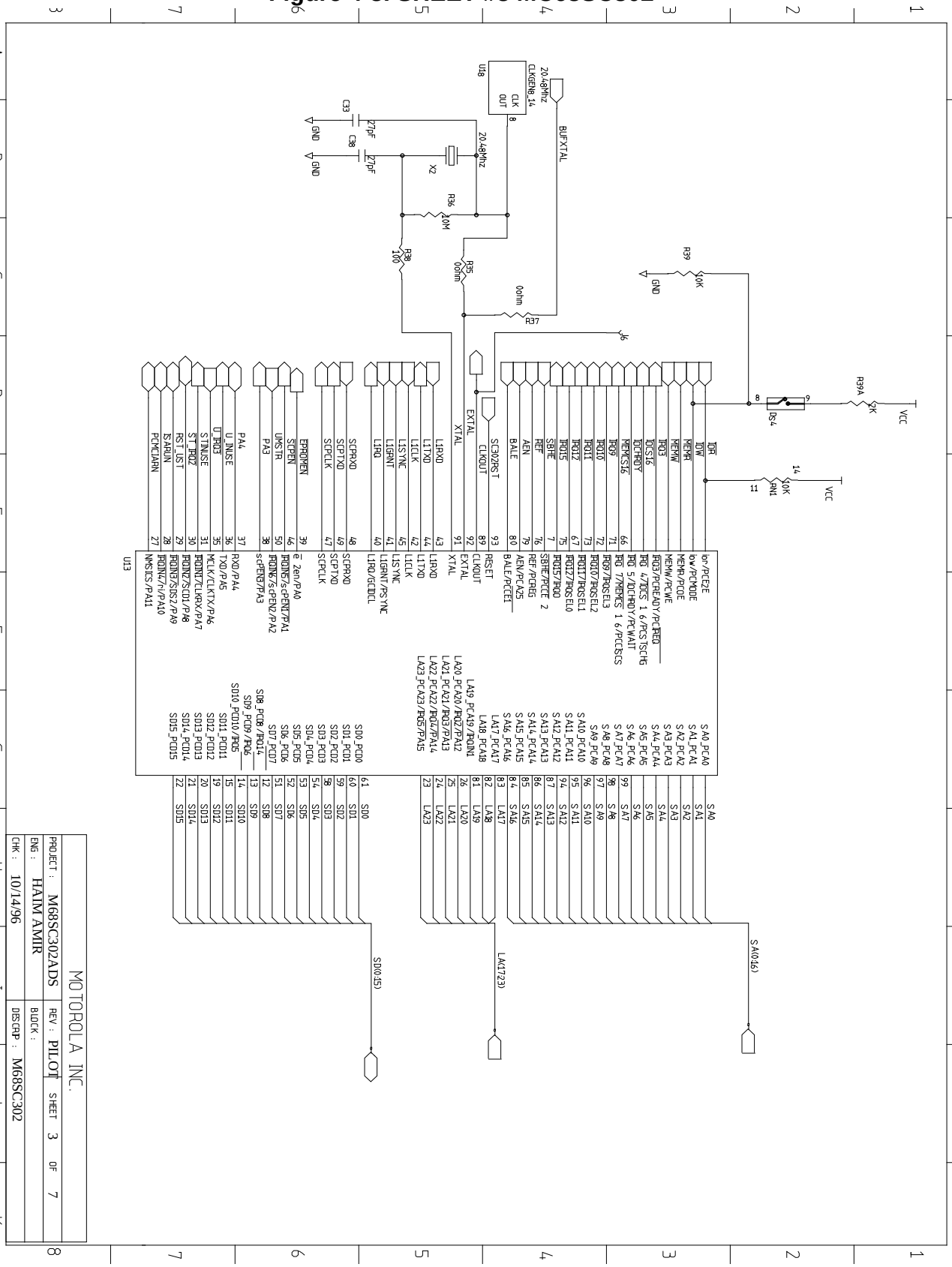
Figure 4-3. SHEET #3 MC68SC302



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4.3 SHEET #3

Sheet #3 shows the MC68SC302. R37 and R35 allow the 68SC302 EXTAL to be driven by either the MC145572 BUFXTAL signal or by crystal (X2). R35 is mounted on the board and R37 is unmounted so the crystal to drives the clock to the SC302. R39 and RN1(11) are made to enable the SC302 to select between ISA and PCMCIA mode.
All of the SC302 pins are connected to the logic analyzer connectors and to the expansion connector.

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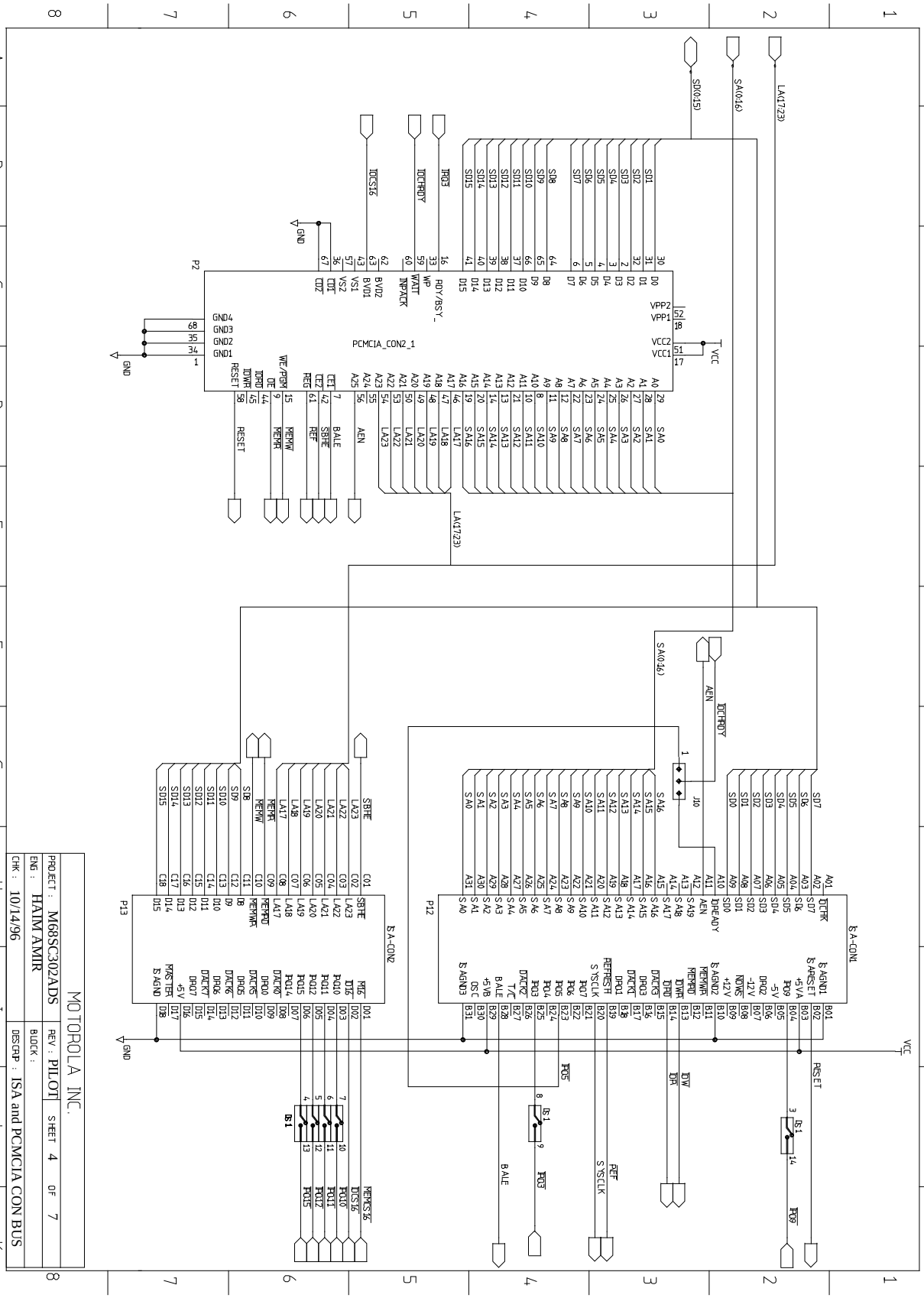
Figure 4-4. SHEET #4 ISA-BUS AND PCMCIA BUS



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4.4 SHEET #4

Sheet #4 shows the ISA and the PCMCIA bus connectors. The SC302 IOCHRD~ signal is muxed with IRQ5~.

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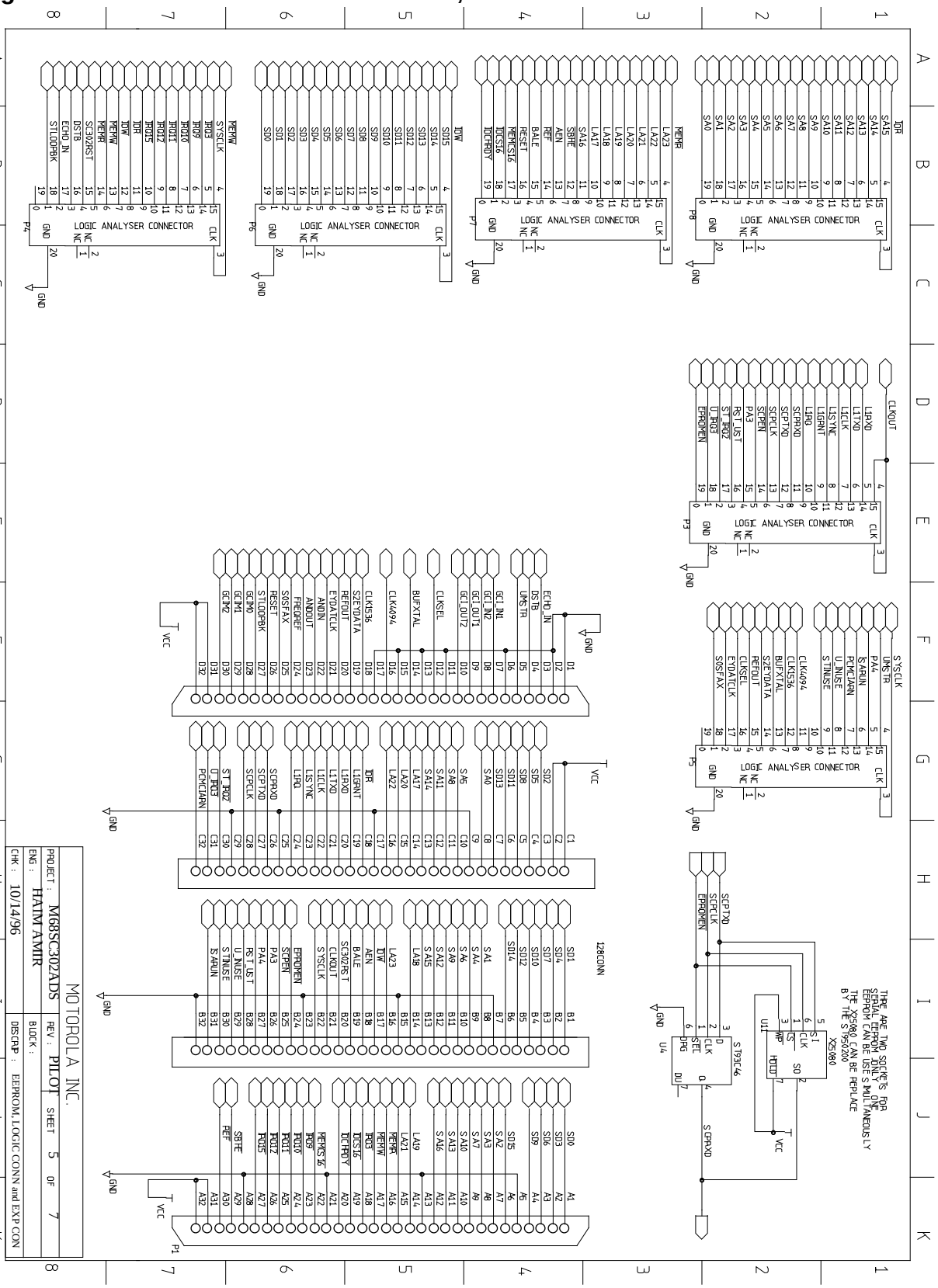
Figure 4-5. SHEET #5 LOGIC ANALYSER, EXPANSION CONNECTERS AND EPROMS



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4.5 SHEET #5

Sheet #5 shows the P3 - P8 logic analyzer connectors to display the SC302 and the necessary pins of the MC145572 and MC145574 pins. P1 is an expansion connector which has all the SC302 pins and the necessary pins of the MC145572 and MC145574 pins for the user applications. Either U4 or U11 will be populated. U11 is for SPI type EEPROMs ST95020 EEPROM or X25080 EEPROM. U4 is ST93C46 EEPROM type.

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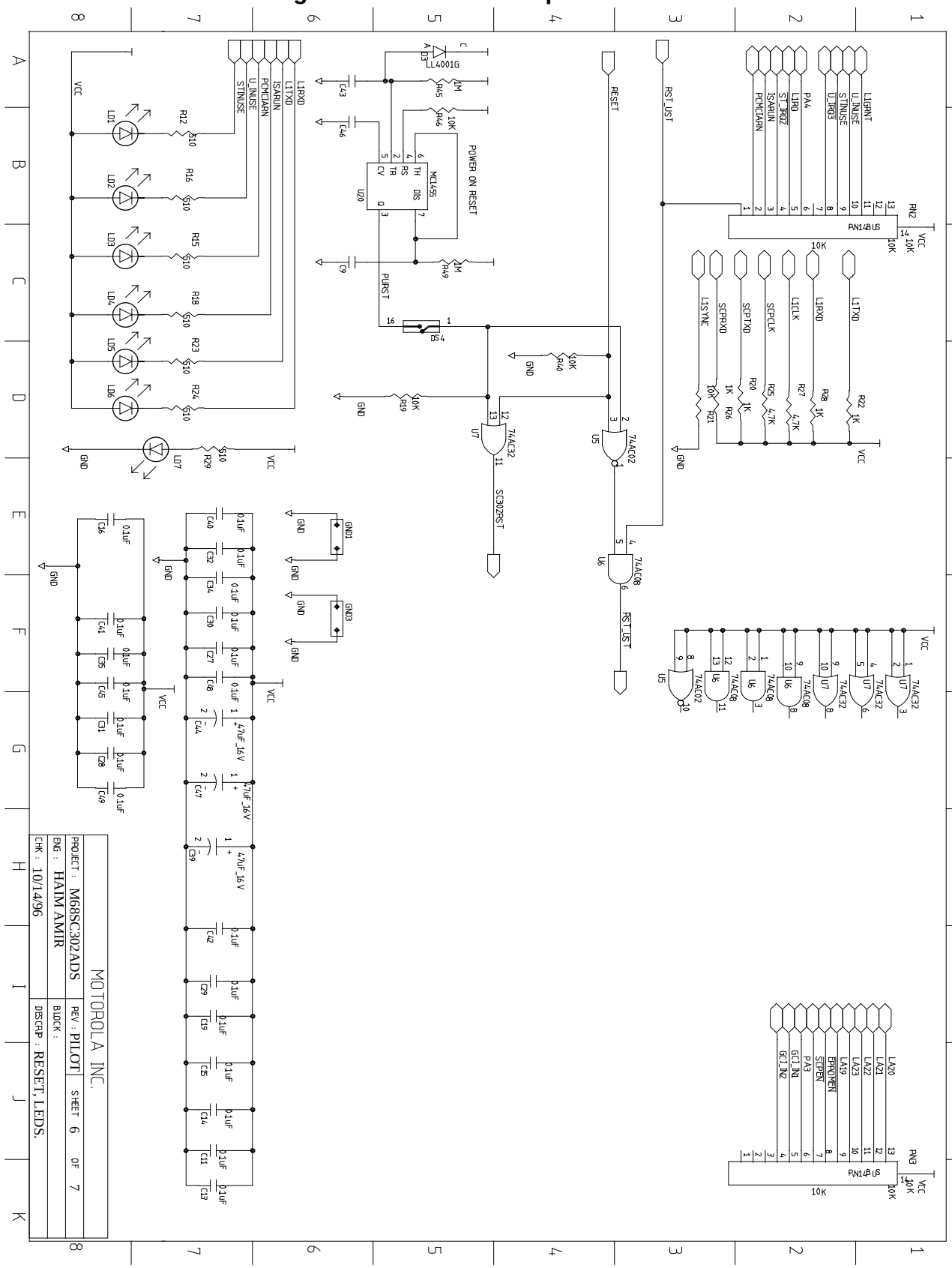
Figure 4-6. RESET Pullups and LEDs



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4.6 SHEET #6

The reset to the SC302 is connected from the ISA bus or from the PCMCIA bus by the RESET signal or from the power up circuit. The power up circuit can be disabled by DS4 (1). The S/T and the U interfaces can be reset from ISA bus, PCMCIA, SC302 or from the power up circuit.The SC302 port pins, The IDL/GCI bus and the SCP busses are pulled up.

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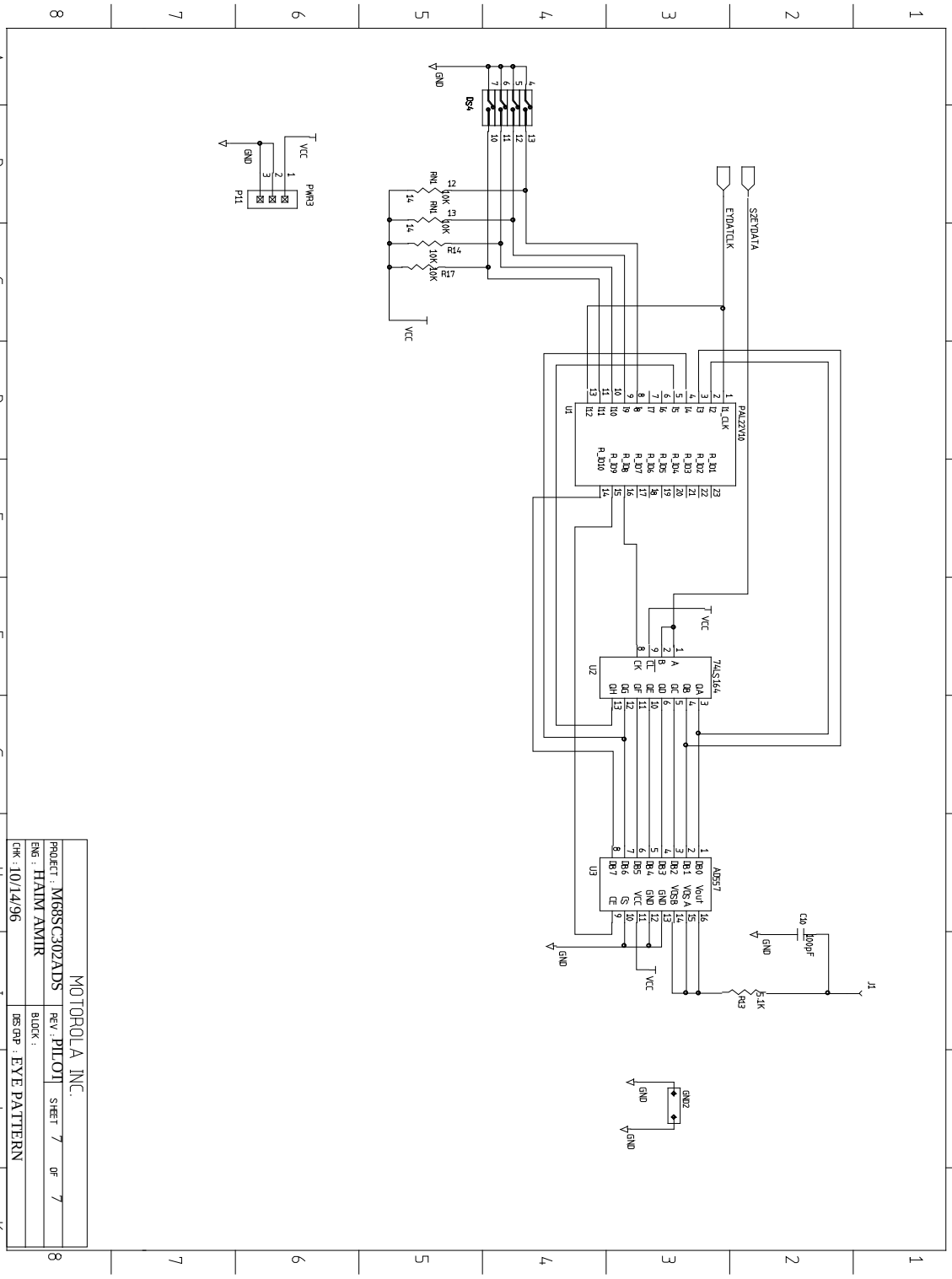
Figure 4-7. SHEET #7 EYE PATTERN DECODER



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4.7 SHEET #7

The EYE Patter Decoder was copied from the MC145572 U interface date sheet and is not populated at the factory. For more information refer to Appendix D in the MC145572 User's Manual.

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SECTION 5
SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the interconnection signals and the parts list of the M68SC302ADS board.

5.2 INTERCONNECT SIGNALS

The M68SC302ADS board interconnects with external devices through the following connectors:

- P1 is a 128 pin, female, expansion connector providing all the signals of the SC302 and most of the MC145572 and MC145574 signals for connection to the user hardware application.
- P2 is a 68 pin female connector to connect the SC302 board to a master PCMCIA board.
- PD3 - PD8 are 20 pin, male connectors that provides all the signals of the master SC302 for bus monitoring.
- P9 is 8 pin, RJ-45 connector, for ISDN U interface analog signals to connect to ISDN line.
- P10 is 8 pin, RJ-45 connector, for ISDN S/T interface analog signals to connect to ISDN line.
- P11 is 3 pin connector for 5v power supply input: 2 GND pins and +5V pin
- P12 and P13 are the ISA Bus edge connectors which are part of the board

Table 5-1 M68SC302ADS Parts List

Reference	Value/PART_NUM	Manufacture	Total
C1	1uF		1
C11 C12 C13 C14 C15 C16 C19 C27 C28 C29 C30 C31 C32 C34 C35 C36 C37 C40 C41 C42 C43 C45 C46 C48 C49	0.1uF		25
C2 C17 C18 C20 C21 C22 C26	0.1uF		7
C3	10uF_16V		1
C4 C6 C23 C24	220nF_200V		4
C5	120nF_200V		1
C7 C8	33pF		2
C9	0.47UF		1
C10	100pF		1
C25	0.015uF		1

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Reference	Value/PART_NUM	Manufacture	Total
C33 C38	27pF		2
C39 C44 C47	47uF_16V		3
D1 D2	1N5232B	MOTOROLA	2
D3 D4 D5	LL4001G		3
DS1 DS2 DS3 DS4	90HBW08S	GRY HILL	4
J2 J5 (J3 J4)	TSM102030SDV	SAMTEC	3
J7 J8 J9 J10	10303SSV	SAMTEC	4
J7 J8 J9 J10 J3 J4 J2 J5	jumper bridge		8
LD1 LD2 LD3 LD4 LD5 LD6 LD7 LD8	LGT679-C0	SIMENS	8
P1 (WW) Male	013175	ERNI	1
P1 Female	043326	ERNI	1
P2	SCD-KS68CA	ITT	1
P3 P4 P5 P6 P7 P8	LPH20SASG	KCC	6
P9 P10	555764-1	AMP	2
P11	253200353	Wieland Bamberg	1
P11	253303353	Wieland Bambe	1
R1 R2	33.2_1%		2
R3 R5 R13	5.1K_5%		3
R4 R8 R38	100		3
R6 R7	64.9_1%		2
R10 R35	0ohm		2
R11 R36	10M		2
R12 R15 R16 R18 R23 R24 R29R30 R41R42 R43 R44 R47 R48	510ohm		14
R14 R17 R19 R21 R34 R39 R40	10K		9
R46 R32			
R20 R22 R26 R28	1K		4
R25 R27	4.7K		2
R31	100K		2
R33	30.1K_1% 30K_5%		1
R45 R49	1M		2
RN1 RN2 RN3	10K		3

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Reference	Value/PART_NUM	Manufacture	Total
TR1 TR2	7.5ohm		2
U1 (SOCKET)	PAL22V10		1
U1	SOCKET		1
U2	74LS164	MOTOROLA	1
U3	AD557	ANALOG DEVICE	1
U4 (SOCKET)	ST93C46	SGS-TOMSON	1
U5	74AC02	MOTOROLA	1
U6	74AC08	MOTOROLA	1
U7	74AC32	MOTOROLA	1
U8	MC145572TQ	MOTOROLA	1
U9	PE68628	Pulse Engineering	1
U10	P1300EA70	Pulse Engineering	1
U11 (SOCKET)	X25080	Xicor	1
U12 U19	MMAD1108	MOTOROLA	2
U13	MC68SC302TQ	MOTOROLA	
U13 (SOCKET)	SOCKET		1
U14	MC145574DW	MOTOROLA	1
U15	PE65798	Pulse Engineering	1
U16 U17	PE65857	Pulse Engineering	2
U18 (SOCKETONLY)	20.48Mhz		1
U20	MC1455	MOTOROLA	1
X1 X2	20.48Mhz MSC-1364	MSC phone number (714) 433-4510	2
X3	15.36Mhz		1

5.3 NETLIST

AEN P1(B18) P2(56) P7(13) P12(A11) U13(79);

ANDIN DS3(12) P1(D22) U14(9);

ANDOUT DS3(13) P1(D23) U14(8);

BALE P1(B19) P2(7) P7(15) P12(B28) U13(80);

BUFXTAL P1(D14) P5(13) R37(1) U8(21);

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CLK1536 P1(D18) P5(12) U8(18);

CLK4094 P1(D16) P5(11) U8(17);

CLKOUT J6(1) P1(B21) P3(3) P3(4) R9(1) U13(89);

CLKSEL DS2(7) P1(D12) P5(16) R32(2) U8(24);

DSTB DS3(16) P1(D4) P4(16) RN1(9) U14(6);

ECHO_IN DS3(7) P1(D3) P4(17) RN1(10) U14(10);

EPROMEN~ P1(B24) P3(19) RN3(8) U4(1) U11(1) U13(39);

EXTAL R35(2) R37(2) U13(92);

EYDATCLK P1(D21) P5(17) U1(1) U1(13) U8(8);

FREQREF P1(D24) U8(25);

GCIM0 J7(2) P1(D28) RN1(5) U14(15);

GCIM1 J8(2) P1(D29) RN1(6) U14(16);

GCIM2 J9(2) P1(D30) RN1(7) U14(17);

GCI_IN1 DS2(13) P1(D7) RN3(5) U8(4);

GCI_IN2 DS2(14) P1(D8) RN3(4) U8(3);

GCI_OUT1 DS2(15) P1(D9) U8(1);

GCI_OUT2 DS2(16) P1(D10) U8(2);

IOCHRDY~ J10(2) P1(A20) P2(59) P7(19) U13(74);

IOCS16~ P1(A19) P2(63) P7(18) P13(D02) U13(65);

IOR~ P1(C18) P4(11) P8(3) P12(B14) RN1(11) U13(77);

IOW~ P1(B17) P4(12) P6(3) P12(B13) R39(1) U13(78);

IRQ3~ DS1(9) P1(A18) P2(16) P4(5) U13(64);

IRQ5~ J10(1) P12(B23);

IRQ9~ DS1(14) P1(A23) P4(6) U13(71);

IRQ10~ DS1(10) P1(A24) P4(7) U13(72);

IRQ11~ DS1(11) P1(A25) P4(8) U13(73);

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IRQ12~ DS1(12) P1(A26) P4(9) U13(67);

IRQ15~ DS1(13) P1(A27) P4(10) U13(75);

ISARUN P1(B31) P5(6) R18(2) RN2(3) U13(28);

L1CLK P1(C22) P3(7) R27(1) U8(14) U13(42) U14(12);

L1GRNT DS3(4) P1(C19) P3(9) RN2(11) U13(41);

L1RQ DS3(5) P1(C24) P3(10) RN2(5) U13(40);

L1RXD P1(C20) P3(5) R24(2) R28(1) U8(13) U13(43) U14(14);

L1SYNC P1(C23) P3(8) R21(1) U8(10) U13(45) U14(11);

L1TXD P1(C21) P3(6) R22(1) R23(2) U8(12) U13(44) U14(13);

LA17 P1(C14) P2(46) P7(10) P13(C08) U13(83);

LA18 P1(B14) P2(47) P7(9) P13(C07) U13(82);

LA19 P1(A14) P2(48) P7(8) P13(C06) RN3(9) U13(81);

LA20 P1(C15) P2(49) P7(7) P13(C05) RN3(13) U13(26);

LA21 P1(A15) P2(50) P7(6) P13(C04) RN3(12) U13(25);

LA22 P1(C16) P2(53) P7(5) P13(C03) RN3(11) U13(24);

LA23 P1(B16) P2(54) P7(4) P13(C02) RN3(10) U13(23);

MEMCS16~ P1(A22) P7(17) P13(D01) U13(66);

MEMR~ P1(A16) P2(9) P4(14) P7(3) P13(C09) U13(8);

MEMW~ P1(A17) P2(15) P4(13) P4(3) P13(C10) U13(9);

PA3 DS2(4) P1(B26) P3(15) RN3(6) U13(38);

PA4 P1(B27) P5(5) RN2(6) U13(37);

PCMCIARN P1(C32) P5(7) R15(2) RN2(2) U13(27);

PURST DS4(16) U20(3);

REFOUT P1(D20) P5(15) U8(23);

REF~ P1(A30) P2(61) P7(14) P12(B19) U13(76);

RESET P1(D26) P2(58) P7(16) P12(B02) R40(1) U5(3) U7(12);

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RST_UST P1(B28) P3(16) RN2(1) U6(4) U13(29);

RST_UST~ U6(6) U8(41) U14(28);

S0SFAX P1(D25) P5(18) R31(2) U8(9);

S2EYDATA P1(D19) P5(14) U2(1) U2(2) U8(22);

SA0 P1(C8) P2(29) P8(19) P12(A31) U13(6);

SA1 P1(B8) P2(28) P8(18) P12(A30) U13(5);

SA2 P1(A7) P2(27) P8(17) P12(A29) U13(4);

SA3 P1(A8) P2(26) P8(16) P12(A28) U13(3);

SA4 P1(B9) P2(25) P8(15) P12(A27) U13(2);

SA5 P1(C10) P2(24) P8(14) P12(A26) U13(1);

SA6 P1(B10) P2(23) P8(13) P12(A25) U13(100);

SA7 P1(A9) P2(22) P8(12) P12(A24) U13(99);

SA8 P1(C11) P2(12) P8(11) P12(A23) U13(98);

SA9 P1(B11) P2(11) P8(10) P12(A22) U13(97);

SA10 P1(A10) P2(8) P8(9) P12(A21) U13(96);

SA11 P1(C12) P2(10) P8(8) P12(A20) U13(95);

SA12 P1(B12) P2(21) P8(7) P12(A19) U13(94);

SA13 P1(A11) P2(13) P8(6) P12(A18) U13(87);

SA14 P1(C13) P2(14) P8(5) P12(A17) U13(86);

SA15 P1(B13) P2(20) P8(4) P12(A16) U13(85);

SA16 P1(A12) P2(19) P7(11) P12(A15) U13(84);

SBHE~ P1(A29) P2(42) P7(12) P13(C01) U13(7);

SC302RST P1(B20) P4(15) U7(11) U13(93);

SCPCLK DS2(3) J9(1) P1(C28) P3(13) R25(1) U4(2) U11(6) U13(47);

SCPEN~ P1(B25) P3(14) RN3(7) U13(46) U14(18);

SCPRXD DS2(1) J7(1) P1(C26) P3(11) R26(1) U4(4) U11(2) U13(48);

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SCPTXD DS2(2) J8(1) P1(C27) P3(12) R20(1) U4(3) U11(5) U13(49);

SD0 P1(A1) P2(30) P6(19) P12(A09) U13(61);

SD1 P1(B1) P2(31) P6(18) P12(A08) U13(60);

SD2 P1(C3) P2(32) P6(17) P12(A07) U13(59);

SD3 P1(A2) P2(2) P6(16) P12(A06) U13(58);

SD4 P1(B2) P2(3) P6(15) P12(A05) U13(54);

SD5 P1(C4) P2(4) P6(14) P12(A04) U13(53);

SD6 P1(A3) P2(5) P6(13) P12(A03) U13(52);

SD7 P1(B3) P2(6) P6(12) P12(A02) U13(51);

SD8 P1(C5) P2(64) P6(11) P13(C11) U13(12);

SD9 P1(A4) P2(65) P6(10) P13(C12) U13(13);

SD10 P1(B4) P2(66) P6(9) P13(C13) U13(14);

SD11 P1(C6) P2(37) P6(8) P13(C14) U13(15);

SD12 P1(B5) P2(38) P6(7) P13(C15) U13(19);

SD13 P1(C7) P2(39) P6(6) P13(C16) U13(20);

SD14 P1(B6) P2(40) P6(5) P13(C17) U13(21);

SD15 P1(A6) P2(41) P6(4) P13(C18) U13(22);

STINUSE P1(B30) P5(9) R12(2) RN2(9) U13(31);

STLOOPBK P1(D27) P4(18) U5(6) U5(5) U14(19);

ST_IRQ2~ P1(C30) P3(17) RN2(4) U13(30) U14(20);

SYSCLK P1(B22) P4(4) P5(3) P12(B20);

UMSTR P1(D5) P5(4) U5(13) U8(43) U13(50);

U_INUSE P1(B29) P5(8) R16(2) RN2(10) U13(36);

U_IRQ3~ P1(C31) P3(18) RN2(8) U8(44) U13(35);

VCAP3 C1(1) U8(28);

XTAL R38(2) U13(91);

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SECTION 6
SPECIFICATIONS

The M68SC302ADS specifications are given in Table 1-1.

Table 5-2

CHARACTERISTICS	SPECIFICATIONS
Power requirements (no other boards attached)	+5Vdc @ 2 A (typical), 2.5 A (maximum)
Operating temperature	0 degrees to 30 degrees C ambient air temperature
Storage temperature	-25 degrees to 85 degrees C
Relative humidity	5% to 90% (non-condensing)
Dimensions Height Depth Thickness	 4.53inches (115 mm) 12.6 inches (320 mm) 0.063 inches (1.6 mm)

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